

The Challenge

In current nano-scale CMOS process technologies and sophisticated automotive process technologies the design and verification effort for mixed-signal circuits is disproportionately increasing. Design rule complexity is exploding and catalogs of case by case design guidelines for different process options have to be considered by the design engineers in order to secure challenging circuit operating conditions, yield, reliability, power limits and quality requirements. The majority of today's available industrial EDA platforms for analog circuit design are addressing most relevant design aspects but unfortunately with a minor degree of task automation and also without navigation support through complex mixed-signal design flows. Everything is easy if the designer is aware about a universe of accompanying constraints and gets not tired in repeating same type of complex manual procedures again and again. Designers questions e.g. on how to import and re-specify a existing design database (schematics, layout, symbols, testbenches, constraint settings) into a new process design kit, or how to automatically consider updated design rules for improved yield in an already completed layout, or how to increase the flexibility and automation degree of the analog engineering process in general remain unanswered cannot for these platforms. Quality assurance processes are not supported in a way that guides designers towards successful design sign offs within given time and cost scheduling.

Our Solution

The **1Stone**® Product Family, offered by IPGEN Microelectronics, strengthens the capabilities of available design frameworks towards design reuse and automation, without leaving existing database formats, qualified PDKs or the trusted design framework and embedded tools. IPGEN Microelectronics provides a cutting-edge, silicon-proven design automation solution that substantially reduces development effort for analog IP's and enhances quality and design security significantly. The **1Stone**® Product Family especially addresses full-custom mixed-signal IP design (schematic, layout, model, testbench) and IP reuse through different applications (specification adjustment) and across multiple technology processes. Designers are enabled to accelerate their design tasks considering individual best practices in their trusted design environment. As a unique feature, the actual engineering result (includes also the layout view) and considered design assumptions remain adaptable to later design update requests (e.g. process shrink, design optimization, specification updates). Complete engineering steps can be documented in an executable manner and re-repeated considering updated conditions, if necessary.

Table 1: **1Stone**® Product Family

1STONE Products	Simulator/ Optimizer	Testbench	Schematic	Layout	PDK +	Process/Platform Porting
1Stone Developer	X	X	X	X	X	X
Schematic Wizard	X	X	X			X
Layout* Processor				X		X
GEMGUI				X	X	X
GEM IP-Library	X	X	X	X	X	X
PCP Device Library				X	X	X
TsF Technology Setup	X	X	X	X	X	X

PCP: Parameterizable for performance, Configurable for application, Portable to process
 GEM: Generic Engineering Model
 TsF: Technology specification File
 PDK: Process Design Kit

Methodology: Design Abstraction and Refinement

Fig. 1 (left column) shows an exemplary work platform configuration which is qualified for efficient analog circuit design processes. IPGEN Microelectronics proposes an extension (right column Fig. 1) assisting designers in managing complex design tasks as design porting and re-specification. The main idea here is to spend special attention to the IP engineering process itself instead of looking mainly to the result of it. Design parameters, PDK selections and even design frameworks can be exchanged easily during the IP engineering process. The professional IP development platform **1Stone**[®]-Developer acts as a complementary extension to available Mentor or Cadence based design frameworks. It completes a future oriented design flow addressing design flexibility down to final layout by adding *symbolic design abstraction* and *synthesis-like design refinement* as mandatory design automation features. An executable testbench secures design consistency between behavioral model, schematic and layout views which are partly addressing tools of different vendors.

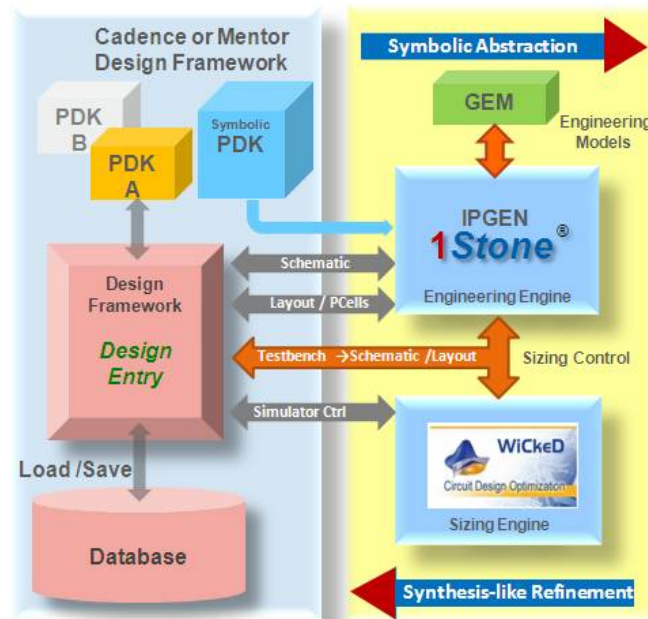


Fig.1: Exemplary Work Environment for secured and portable Analog Circuit Design

The symbolic *design abstraction* step includes transforming of complex analog and mixed-signal designs into compact symbolic design descriptions, taking the complete engineering process and design flow interaction into account. The GEM approach especially transforms and abstracts the complex geometries on layout level as well as design guidelines into soft properties for a unified symbolic layout view. After a transformation operation the analog design description is optimized for a language based processing.

For re-use purpose the abstraction process has to be reversed. The synthesis-like *design refinement* step enables individual constraint and fabrications process mapping. Since optimal IP sizing depends on the available process models as well as updated specifications, optimization and sizing usually does not follow given algorithms. In the given example the circuit optimizer WiCkeD (MunEDA) enriches the refinement flow in a way that takes advantage of given testbench and described layout characteristics. **1Stone**[®] takes care of WiCkeD setup parameters since all IP details related to schematic, layout and testbenches are documented within the existing GEM description. The proposed combination of **1Stone**[®]-Developer and WiCkeD assist designers in finding a tailored layout solution starting from a given specification and a pre-sized schematic. Recently missing consistency of layout, model and technology constraints has been a real design efficiency and performance limiter. In the proposed work flow the number of required control parameters can be reduced and contradicting redundancy is omitted. Example: Matching characteristics in standard device models are not able to consider enhanced layout techniques (e.g. common centroid, statistical averaging, optimized interconnects with reduced parasitics) which can be applied in special cases. GEM descriptions include self-adapting layout information which corresponds to given schematics and sizing information. If necessary, the available device models are calibrated according to selected layout techniques.

Take the offered Highway to reach your Sign Off

1Stone® tools are assisting from background and take care about design flow management, PDK-rule and -device administration and consistency of constraints in different views (e.g. schematic, layout, behavioral model, optimizer, backannotated parasitics).

You should have a closer look at our EDA solution in case you are planning to:

- **Reuse complex designs** from an older process node
- **Automate repetitive tasks** (application, process, configuration may change) and **develop room for the innovative ones**
- Offer your **Analog-IPs** also in additional fabrication processes and **develop new markets**
- **Extend and automate** existing time and resource consuming design **optimization loops across layout** (yield, reliability, sizing) and **increase reliability**
- Convert your successful but inflexible designs into a **configurable and portable module or device generators** and avoid new developments from the scratch
- Ramp up a powerful **process independent analog library** (e.g. interface circuits, built-in-self-test, built-in-self-calibration) in order to increase your productivity
- Apply algorithmic techniques also for **advanced schematic and layout creation** (e.g. address techniques for self calibration, defect tolerance, shielding, improved device features, self-sizing)
- Implement a **automated Failure Mode and Effects Analysis (FMEA)** system for security relevant applications (e.g. automotive, health)
- Realize complex **process/device characterization structures and intelligent arrays** with or without embedded testing support in the area of process technology development (PCM, SLM)
- Search for customized EDA platform solutions that support your specific **quality assurance processes**
- Reduce you verification and optimization effort by using a **testbench template approach** with tailored test pattern generation/result evaluation which also enables **yield estimation and optimization** functionality

Please contact us for more details and reserve a time slot for an individual product presentation, which is addressing your specific needs!