

GEM: Digital Controlled Potentiometer

Datasheet and Samples

Keywords: Analog-to-Digital Converter (ADC), Digital-to-Analog Converter (DAC), Digital Controlled Potentiometer (DCP), Successive Approximation Register ADC (SAR-ADC), Resistive DAC (RDAC), Potentiometer DAC (PDAC), IQ DAC

Application Areas: Analog Signal Processing, Sensing, Wired Solutions, Wireless, Video, Instrumentation, DC Signal Referencing, Automotive, Telecommunications

DCP Topologies: DCP, DAC, ADC, Analog Precision Divider

Silicon Proven: CMOS/BiCMOS for Automotive & Telecommunications
Structure Sizes: 65nm, 130nm, 350nm, 600nm, 800nm

SOI Structure Size: 0.5 μm

for resolutions in Bit: 8, 9, 10, 12, 14, 15

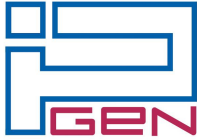
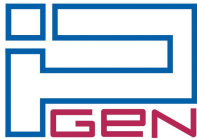


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1. KEY CHARACTERISTICS

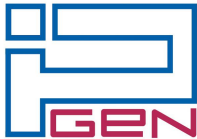
Resolution:	4 to 16 bit
Operating Speed:	DC up to 500MHz (clock rate)
Coding:	Binary offset (other schemes by request)
Output:	Single ended
Target Process Technologies:	CMOS / BiCMOS / SOI from 0.8 μm down to 40nm
Process Porting Capability:	Yes
Signal Processing:	full parallel
Data Interface:	serial or parallel
Temperature Range:	consumer, industrial, automotive
Channels:	single, dual matched (IQ), triple matched (opportunity), matched multi-channel (opportunity)

2. GDS2 DELIVERY (TAPE OUT)

GEM IP can be compiled into any CMOS Process with a substantial device library (Mentor and Cadence PDK has to be available !)

Initial Process Node Design (typical): 6-8 Weeks (Specification to Tape-Out)

Known Process Node Design (typical): 4-6 Weeks (Specification to Tape-Out)



3. SPECIFIC ARCHITECTURE FEATURES

- Monotonic by construction
- Low temperature sensitivity
- Long term stability
- Statistical Averaging Principle (parameter variations do not degrade linearity, DFY)
- DC Mode (0 Hz clock operation, storage mode)
- Full parallel signal processing
- No analog process options required

4. IP DESCRIPTION

A flexible Executable Engineering Model (GEM) is available to adapt this IP to individual requirements (Generic Engineering Model, see also www.ipgen.de). Flexibility includes resolution, resistance of voltage divider, clock rate, area, aspect ratio, linearity, supply voltage, reference voltages, target process technology.

Fig. 1 shows the block diagram of the basic **Digital Controlled Potentiometer** IP. R-String1 consists of 2^N high precision resistors, providing high accurate reference node voltages. This R-String determines the overall accuracy of the DCP. Therefore the area of each single unit resistor is large to achieve a small standard deviation. Furthermore R-String1 has low-impedance, determining the driving capability of the overall DCP. R-String2 consists of 2^N sub chains of 2^{M-N} serial low precision unit resistors (2^M unit resistors in total). Each of the single R-String2 sub chains is attached to one R-String1 resistor. The area efficiency of R-String2 topology can be increased strongly using small unit resistors with poor standard deviation. This DCP topology enables an area and power efficient design, as one R-String of the DCP is fully in charge of overall accuracy and driving capability utilizing traditionally large low-impedance unit resistors, and the other R-String has relaxed accuracy requirements and provides the needed voltage nodes using very small unit resistors.

The basic DCP shown in Fig.1 can be configured to different topologies by adding a few additional components. Therefore the DCP is easily extendable to a DAC (Fig.2), ADC (Fig. 3) or it also can be arranged to build an Analog Precision Divider (again Fig. 1 using performance matched resistors).

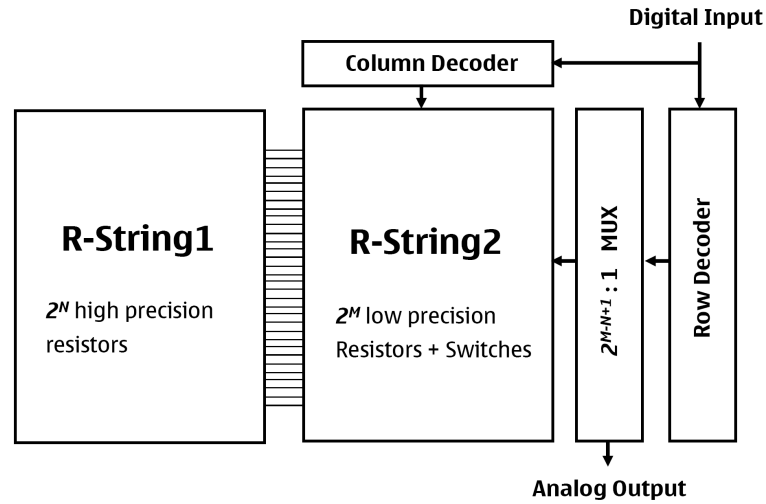


Figure 1: Block diagram of the basic DCP architecture and the Analog Precision Divider

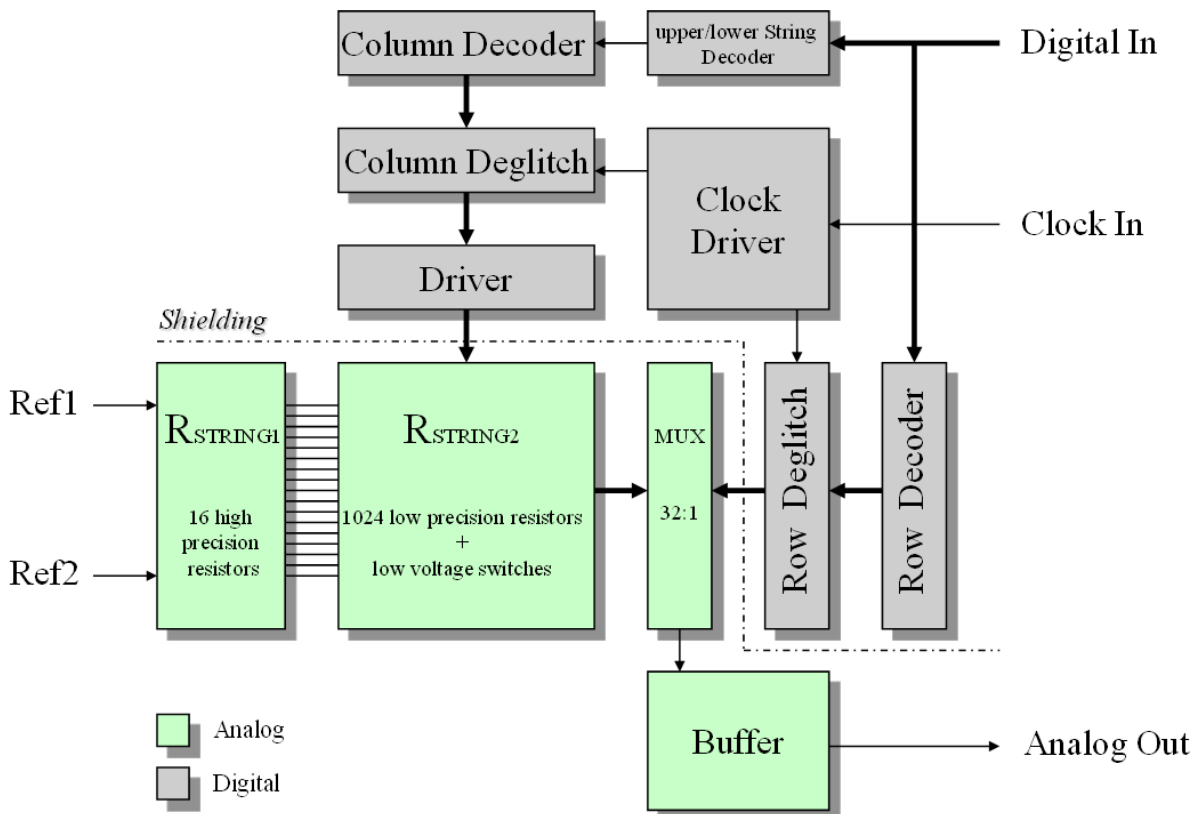


Figure 2: Extension of the DCP architecture to form a high speed DAC (Example 10bit)

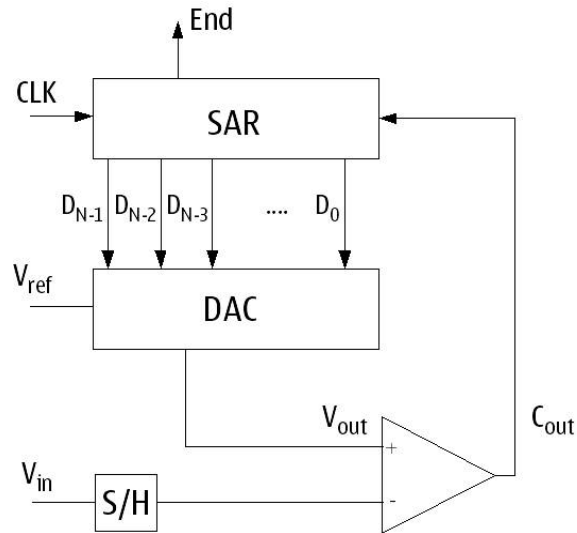


Figure 3: Extension of the DCP/DAC architecture to form an n-bit SAR ADC

5. DESIGN-FOR-YIELD MODEL

Fig. 4 shows an example of the modeled yield of a 12 bit DCP as a function of the unit resistor tolerances of R-String1 and R-String2. The yield dependency has to be considered during the design optimization cycle. The black square in the plots shows the indirectly measured yield point based on estimations of the standard deviations of the measured unit resistors of both R-Strings. This result shows the optimization potential of the DCP in terms of area efficiency, as the unit resistor tolerances of both R-Strings could be smaller without degrading the yield performance of 100%, leading to a smaller physical size of the DCP layout area. A safety margin should be defined to take other technology related variations into account.

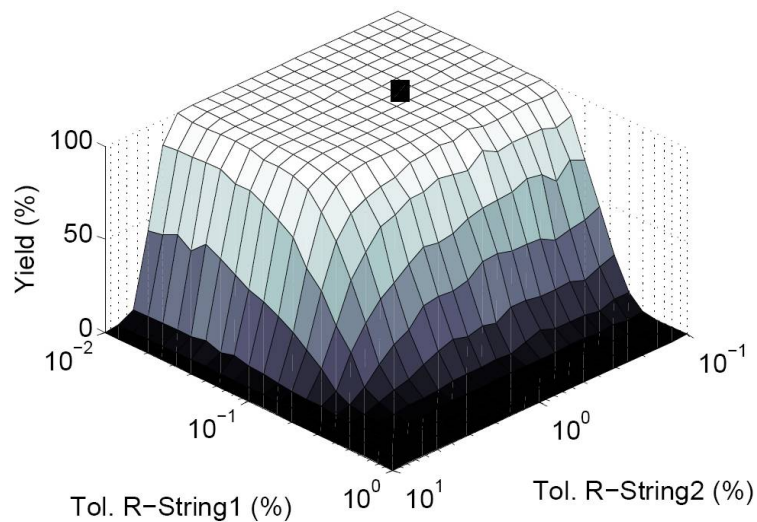
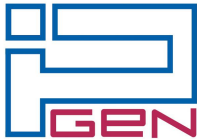


Figure 4: Yield as function of $\sigma_{R-String1}$ and $\sigma_{R-String2}$



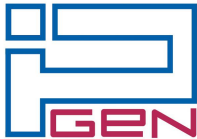
6. APPLICATION EXAMPLES

a) DCP Application

Three different DCP IP compilations into two different process technologies have been fabricated and measured (Table 1). 180nm CMOS is the latest process-node for automotive applications. The measurement results indicate excellent DCP-IP portability capabilities proven by excellent linearity results at block level in presence of changing process environment conditions. The tolerances σ of the unit resistors of R-String1 and R-String2 have been estimated out of the measured node voltages, assuming a constant current through R-String1 and R-String2. Comparing the DCP areas shows a factor of 4 between 12 bit and 14 bit and a factor of approx. 8 between 12 bit/65 nm and 12 bit/180 nm, which is in line with technology scaling principles. The measured standard deviation of R-String2 for the 14bit DAC case is about 3%. This is not critical in this architecture for related INL and DNL values. Comparing the 12 bit DAC accuracy in terms of INL and DNL between 65 nm and 180 nm shows an accuracy improvement after down-scaling, taking the LSB size into account.

Table 1: DCP performance summary

CMOS-Process	DCP		
	65 nm Vendor 1		180 nm Vendor 2
Resolution n [bit]	12	14	12
States $m = 2^n$	4096	16384	4096
LSB= V_{DD}/m [μ V]	293	73	610
INL _{max} average	± 0.446	± 0.95	± 0.332
DNL _{max} average	0.100	0.15	0.073
DAC-Area [mm ²]	0.095	0.38	0.72
Power [μ W] @ V_{DD}	665 @ 1.2V	296 @ 1.2V	740 @ 2.5V
R [Ω]	8.5	9	6.5
R _{String1} : Number of unit resistors	32	128	32
R _{String1} [Ω]	70	38.75	326
R _{String2} : Number of unit resistors	32x128	128x128	32x128
R _{String2} [Ω]	15.2	15	10.5
σ [%] of R _{String1} unit resistors	0.073	0.069	0.0358
σ [%] of R _{String2} unit resistors	0.541	≈ 3	0.387



b) Modem DAC Application

	DAC 1	DAC 2
Resolution	10 bits	12 bits
Conversion Rate	85 MS/s	100 KS/s
Integral Nonlinearity	0.3 LSB	0.8 LSB
Differential Nonlinearity	0.11 LSB	0.15 LSB
SFDR	> 50 dB (0-25 MHz)	> 60 dB (0-50 KHz)
Rise/Fall Time (10-90%)	3.5 ns	-
Power Dissipation	80 mW	20 mW
Supply Voltage	3.3 V	3.3 V
Output Range	0.5 – 1.5 V	0 – 1.7 V
Load	100 Ω / 25 pF	1 M Ω / 15 pF
Process	0.35 μ m CMOS	0.35 μ m CMOS

c) SAR-ADC Application

Linearity (secured monoton, no missing codes):

	INL	DNL	Conditions
8 Bit	0.1 LSB	0.1 LSB	Clk = 3.5 MHz, Vdd=3.3V, Vref0=2.5V, Vref1=80mV
12 Bit	0.8 LSB	0.4 LSB	Clk = 3.5 MHz, Vdd=3.3V, Vref0=2.5V, Vref1=165mV

Transient measurements (THD, SNR)

Input signal: Signal-source THD for 10 kHz signal approx. 74 dB

Signal amplitude: 2 Vpp
 Clock rate: 3.2 MHz
 Sampling rate = Clockrate / 16: 200 kHz,
 Timing equivalent to Clockrate / 13: 250 kHz

8 Bit: SFDR > 62 dB (CLK = 3.2 MHz)
 12 Bit: SFDR > 70 dB (CLK = 3.2 MHz)

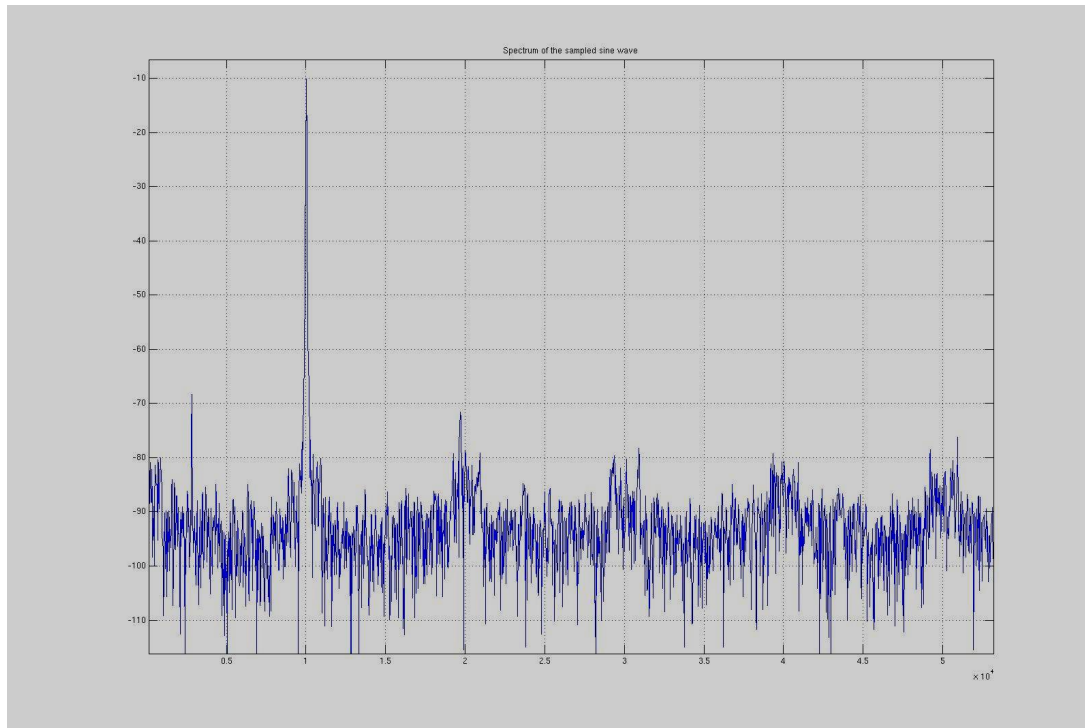
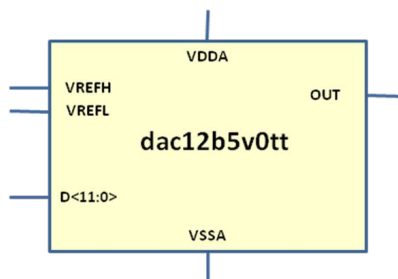


Figure: SFDR measurement result of 8 bit SAR-ADC ($f_{in} = 10$ kHz)

7. DAC IP CATALOG EXAMPLE: DAC12B5V0TT (XFAB XC018)

dac12b5v0tt is a 12-bit voltage-scaling (potentiometric) digital-to-analog converter (DAC). The dac12b5v0tt DAC operates with a single 5,0V power supply and external reference voltage. Physical size (h x w): 920 μm x 780 μm (macro cell) in process XC018

Symbol:

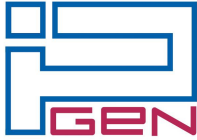


Pin description:

vdd!	digital power supply
VDDA	analog power supply
gnd!	digital ground
VSSA	analog ground
REFH	high reference voltage input
REFL	low reference voltage input
OUT	DAC output

Parameters:

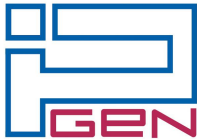
Parameter	Description	min	typ	Max	Unit	Conditions
RES	Resolution		12		Bit	$V_{DD}=5,0V$; $T = -40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$
INL	Integral nonlinearity		1.5	2	LSB	$V_{DD}=5,0V$; $T = -40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$
DNL	Differential nonlinearity		0.2	0.4	LSB	$V_{REF}=V_{DD}=5,0V$; $T=25\text{ }^{\circ}\text{C}$
T_{CONV}	Conversion time		0.4		μs	$V_{DD}=5,0V$; $C_{LOAD}=2\text{ pF}$
V_{REFH}	High reference voltage	0	V_{DD}	V_{DD}	V	$V_{DD} = 4,5$ to $5,5V$; $T = -40$ to $85\text{ }^{\circ}\text{C}$
V_{REFL}	Low reference voltage	0	0	V_{DD}	V	$V_{DD} = 4,5$ to $5,5V$; $T = -40$ to $85\text{ }^{\circ}\text{C}$
R_{IN}^*	Resistance of the voltage divider		8		$\text{k}\Omega$	$T=25\text{ }^{\circ}\text{C}$

**Datasheet GEM-IP: Digital Controlled Potentiometer**

C_{LOAD}	Load capacitance		2		pF	$V_{DD} = 5,0V$ $T = -40 \text{ to } 85 \text{ } ^\circ\text{C}$
V_{DD}	Supply voltage	2,7	3,3	3,6	V	$T = -40 \text{ to } 85 \text{ } ^\circ\text{C}$
I_{DD}	Supply current		20	40	μA	$V_{DD}=5,0V; T=25 \text{ } ^\circ\text{C}$

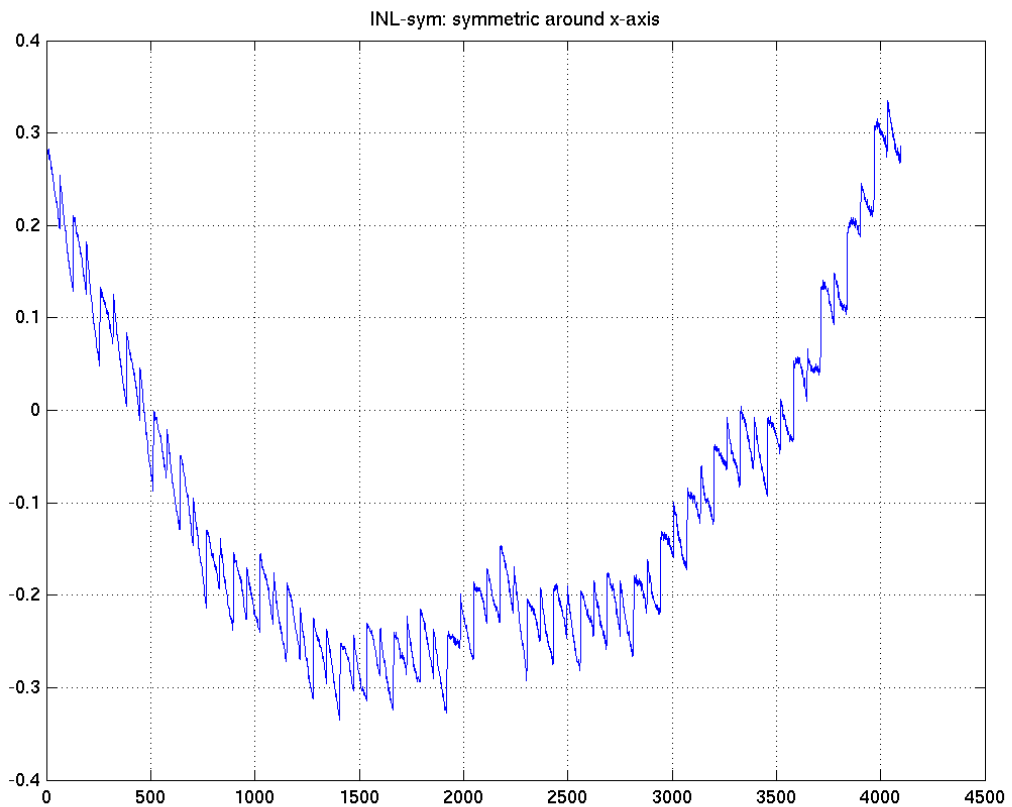
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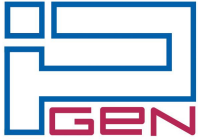
The reference voltage source has to provide the current flowing through the resistive divider.



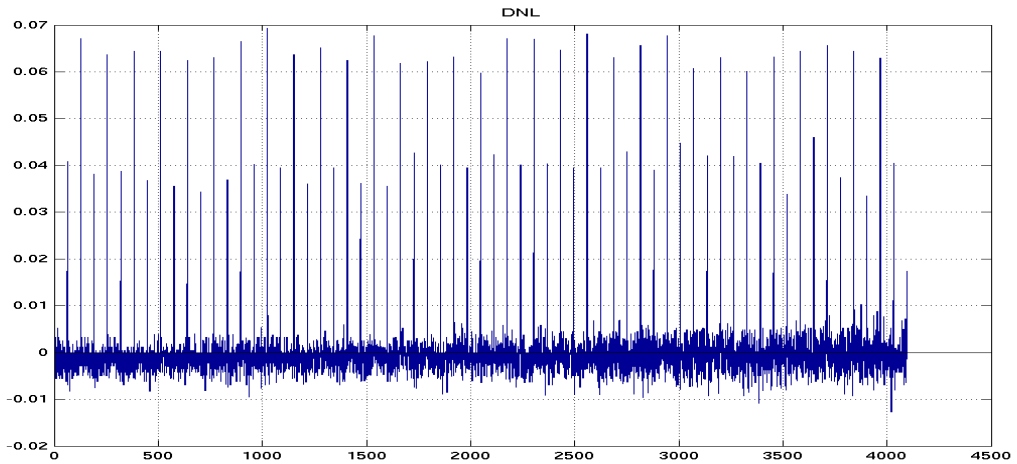
Typical performance characteristics (measured values):

INL versus Input Code ($V_{DD}=5.0V$, $V_{ref}=5.0V$, $T=25^{\circ}C$)

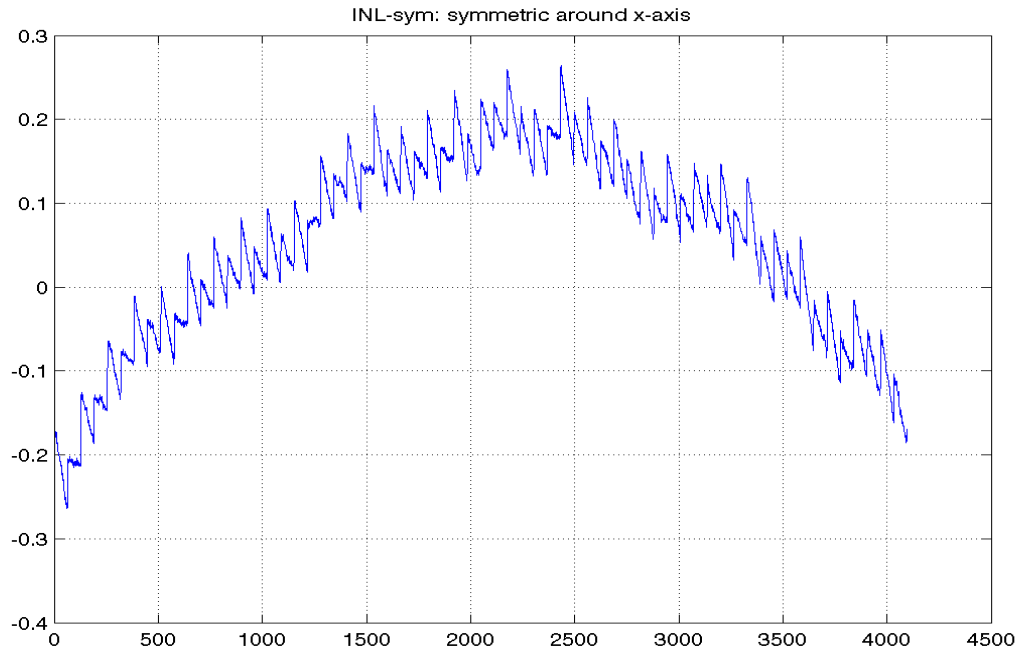


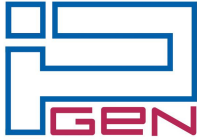


DNL versus Input Code ($V_{DD}=5.0V$, $V_{ref}=5.0V$, $T=25^{\circ}C$)



INL versus Input Code ($V_{DD}=5.0V$, $V_{ref}=2.5V$, $T=25^{\circ}C$)





DNL versus Input Code ($V_{DD}=5.0V$, $V_{ref}=2.5V$, $T=25^{\circ}C$)

